CLAIM LISTING

This listing of claims will replace all prior versions, and listings of claims in the application:

AMENDMENTS TO THE CLAIMS

1.-31. (Cancelled)

32. (Previously Presented) A packaged semiconductor comprising:

a package substrate having an exposed perimeter portion;

a semiconductor integrated circuit mechanically and electrically attached to the package substrate with a ball grid array attachment;

a metal package lid having a sloped wall, a top, and a vent allowing gases to escape during assembly of the packaged semiconductor to a printed circuit assembly;

molding compound applied to only external portions of the exposed perimeter portion of the package substrate and external portions of the sloped wall of the metal package lid so as to secure the package lid to the package substrate; and

thermal grease disposed between the semiconductor integrated circuit and the top of the metal package lid.

33. (New) The packaged semiconductor of claim 32 wherein the sloped wall of the package lid has a slope angle between 30 degrees and 60 degrees.

34. (New) The packaged semiconductor of claim 32 wherein the package lid further comprises a foot around at least a portion of the perimeter of the sloped wall, configured to provide contact between the package substrate and the package lid.

35. (New) The packaged semiconductor of claim 32 wherein the package lid is a stamped package lid.

36. (New) The packaged semiconductor of claim 35 wherein the stamped package lid has a thickness less than 2.39 mm.

37. (New) The packaged semiconductor of claim 35 wherein the stamped package lid has a thickness of about 0.79 mm.

38. (New) The packaged semiconductor of claim 35 wherein the stamped package lid has a thickness between about 0.45 mm and about 2.39 mm.

39. (New) The packaged semiconductor of claim 35 wherein the stamped package lid comprises nickel-plated copper.

40. (New) The packaged semiconductor of claim 32 wherein the package lid further comprises a vent for allowing gases to escape during assembly of the packaged semiconductor to a printed circuit assembly.

41. (New) The packaged semiconductor of claim 40 wherein the vent is provided in a side of the package lid.

42. (New) The packaged semiconductor of claim 40 wherein the vent comprises a gap in the sloped wall.

43. (New) The packaged semiconductor of claim 32 further comprising a rim forming a vertical wall around a top of the package lid.

44. (New) The packaged semiconductor of claim 43 further comprising fiducial marks formed in the rim.

45. (New) The packaged semiconductor of claim 44 wherein the fiducial marks are formed in corners of a rectangular package lid.

46. (New) The packaged semiconductor of claim 32 wherein the package lid is substantially rectangular.

47. (New) The packaged semiconductor of claim 46 wherein the package lid is rectangular and covers a programmable logic device at least 25.4 mm long on a first side.

48. (New) The packaged semiconductor of claim 32 wherein the exposed perimeter portion of the package substrate comprises polymer material.

49. (New) The packaged semiconductor of claim 32 wherein the package lid is disposed on the package substrate to provide the exposed perimeter portion and further comprising:

first molding compound applied to a first portion of the exposed perimeter portion and contacting the sloped sidewall, and

second molding compound applied to a second portion of the exposed perimeter portion and contacting the sloped sidewall, wherein the first portion of the exposed perimeter portion is opposite the second portion of the exposed perimeter portion.

50. (New) The packaged semiconductor of claim 49 wherein the package substrate comprises an organic resin.

51. (New) The packaged semiconductor of claim 49 wherein the package substrate comprises a solder ball-grid array for connecting the packaged semiconductor to a printed circuit assembly.